

SN74LVCZ240A OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS SCES273H-JUNE 1999-REVISED APRIL 2005

FEATURES	DB, DGV, DW, N, NS, OR PW PACKAGE				
Operates From 2.7 V to 3.6 V	(TOP VIEW)				
Inputs Accept Voltages to 5.5 V					
 Max t_{pd} of 6.5 ns at 3.3 V 					
Typical V _{OLP} (Output Ground Bounce)					
< 0.8 V at V _{CC} = 3.3 V, T _A = 25°C	2Y4 [] 3 18 [] 1Y1 1A2 [] 4 17 [] 2A4				
 Typical V_{OHV} (Output V_{OH} Undershoot) 	2Y3 5 16 1Y2				
> 2 V at V _{CC} = 3.3 V, T _A = 25°C	1A3 6 15 2A3				
 I_{off} and Power-Up 3-State Support Hot 	2Y2 [7 14] 1Y3				
Insertion	1A4 [8 13] 2A2				
 Supports Mixed-Mode Signal Operation on 	2Y1 9 12 1Y4				
All Ports (5-V Input/Output Voltage With	GND 11 2A1				
3.3-V V _{cc})					

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCZ240A is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

This device is organized as two 4-bit buffers/drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

T _A	T _A PACKAGE ⁽¹⁾ ORDERABLE F		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP – N	Tube of 20	SN74LVCZ240AN	SN74LVCZ240AN	
-		Tube of 25	SN74LVCZ240ADW	1.1/070404	
	SOIC – DW	Reel of 2000	SN74LVCZ240ADWR	LVCZ240A	
	SOP – NS	Reel of 2000	SN74LVCZ240ANSR	LVCZ240A	
–40°C to 85°C	SSOP – DB	Reel of 2000	SN74LVCZ240ADBR	CV240A	
		Tube of 70	SN74LVCZ240APW		
	TSSOP – PW	Reel of 2000	SN74LVCZ240APWR	CV240A	
		Reel of 250	SN74LVCZ240APWT		
	TVSOP – DGV	Reel of 2000	SN74LVCZ240ADGVR	CV240A	

ORDERING INFORMATION

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LVCZ240A OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

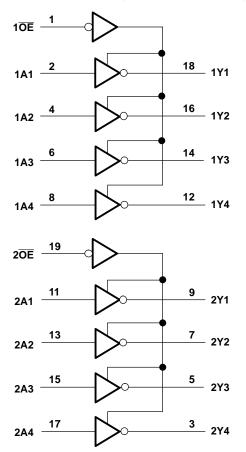
When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE (EACH BUFFER)

INPL	JTS	OUTPUT			
OE	Α	Y			
L	Н	L			
L	L	н			
Н	Х	Z			

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range ⁽²⁾		-0.5	6.5	V
Vo	Voltage range applied to any output in the	high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
Vo	Voltage range applied to any output in the	high or low state ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	
	Continuous current through V_{CC} or GND			±100	mA
	Continuous current through V _{CC} or GND	DB package		70	
		DGV package		92	
0	Declarse thermal impedance (4)	DW package		58	°C/W
θ_{JA}	Package thermal impedance ⁽⁴⁾	N package		69	°C/vv
		NS package		60	
		PW package		83	
T _{stg}	Storage temperature range		-65	150°C	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed. (2)

(3) The value of V_{CC} is provided in the recommended operating conditions table. (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.7	3.6	V
V _{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V		0.8	V
VI	Input voltage		0	5.5	V
Vo	Output voltage	High or low state	0	V_{CC}	V
vo	Output voltage	3-state	0	5.5	v
	Lieb lovel output outpot	$V_{CC} = 2.7 V$		-12	mA
I _{OH}	OH High-level output current	$V_{CC} = 3 V$		-24	mA
1	Low lovel output ourrent	V _{CC} = 2.7 V		12	س ۸
I _{OL}	Low-level output current	$V_{CC} = 3 V$		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			6	ns/V
$\Delta t / \Delta V_{CC}$	Power-up ramp rate		150		μs/V
T _A	Operating free-air temperature		-40	85	°C

All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. (1)

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	NDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT	
	I _{OH} = −100 μA		2.7 V to 3.6 V	V _{CC} - 0.2				
V	10 m		2.7 V	2.2			V	
V _{OH}	$I_{OH} = -12 \text{ mA}$		3 V	2.4			v	
	I _{OH} = -24 mA		3 V	2.2				
	I _{OL} = 100 μA		2.7 V to 3.6 V			0.2		
V _{OL}	I _{OL} = 12 mA		2.7 V			0.4	V	
	I _{OL} = 24 mA		3 V	0.55				
I _I	$V_{I} = 0$ to 5.5 V	3.6 V			±5	μA		
I _{off}	V_{I} or $V_{O} = 5.5 V$		0	±5		μΑ		
I _{OZ}	$V_0 = 0$ to 5.5 V		3.6 V	±5		±5	μΑ	
I _{OZPU}	$V_0 = 0.5$ to 2.5 V,	\overline{OE} = don't care	0 to 1.5 V	±5		±5	μΑ	
I _{OZPD}	$V_0 = 0.5$ to 2.5 V,	\overline{OE} = don't care	1.5 V to 0			±5	μA	
1	$V_{I} = V_{CC}$ or GND	1 0	2.6.1/		100		A	
Icc	$3.6 \text{ V} \le \text{V}_1 \ \le 5.5 \text{ V}^{(2)}$	$I_{O} = 0$	3.6 V	100		μA		
ΔI_{CC}	One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			100	μA	
Ci	$V_{I} = V_{CC}$ or GND		3.3 V		3.5		pF	
Co	$V_0 = V_{CC}$ or GND		3.3 V		5.5		pF	

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.7 V	V _{CC} = ± 0.3	UNIT	
	(INFOT)	(001F01)	MIN MAX	MIN	MAX	
t _{pd}	A or B	B or A	7.5	1.3	6.5	ns
t _{en}	OE	A or B	9	1.1	8	ns
t _{dis}	OE	A or B	8	1.4	7	ns

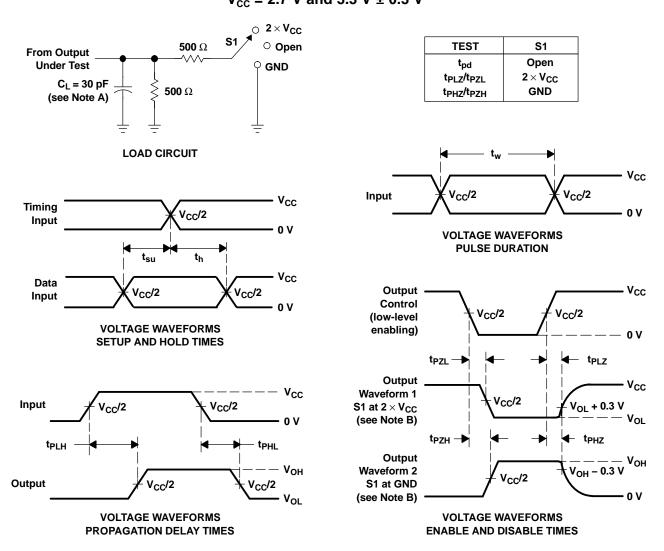
Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 3.3 V TYP	UNIT	
C	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	37	pF	
C _{pd}	Power dissipation capacitance per buner/driver	Outputs disabled		3		

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PARAMETER MEASUREMENT INFORMATION $V_{cc} = 2.7 \text{ V}$ and 3.3 V ± 0.3 V



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. $t_{PLH} \, \text{and} \, t_{PHL} \, \text{are the same as} \, t_{pd}.$
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

4-Jun-2007

PACKAGING INFORMATION

TEXAS INSTRUMENTS www.ti.com

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVCZ240ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240AN	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LVCZ240ANE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LVCZ240ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVCZ240APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM



Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Pa	ackage Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVCZ240APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

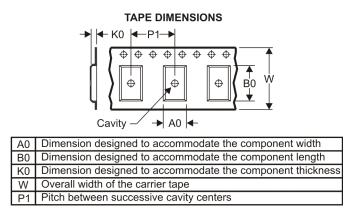
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

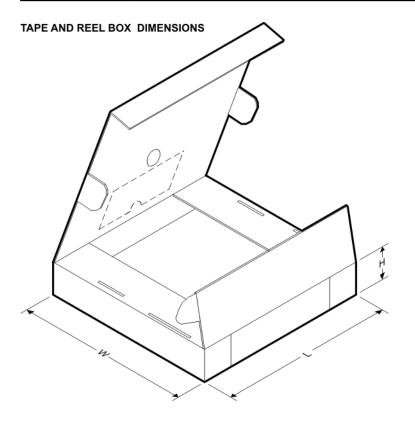


Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCZ240ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVCZ240ADGVR	TVSOP	DGV	20	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LVCZ240ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LVCZ240ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LVCZ240APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

5-Aug-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCZ240ADBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74LVCZ240ADGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
SN74LVCZ240ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LVCZ240ANSR	SO	NS	20	2000	346.0	346.0	41.0
SN74LVCZ240APWR	TSSOP	PW	20	2000	346.0	346.0	33.0

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



MTSS001C - JANUARY 1995 - REVISED FEBRUARY 1999

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



PLASTIC SMALL-OUTLINE

MPDS006C - FEBRUARY 1996 - REVISED AUGUST 2000

DGV (R-PDSO-G**)

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153

14/16/20/56 Pins – MO-194



DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



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